Amendments to the Drawings:

The attached sheets of drawings include changes to Figures 4A, 4B and 5. These sheets replace the original sheets.

Remarks/Arguments:

The present invention relates to a digital signal receiver which includes a signal generator and a base-band transform circuit. Specifically a frequency divider divides a reference signal and a frequency multiplier multiplies the output of the divider.

On page 2 of the Office Action, the Examiner objects to Fig. 5 because it should be designated as "prior art". Applicants have therefore amended Fig. 5 as suggested by the Examiner. The Examiner has also objected to Figs. 4A and 4B because there are no labels for the blocks. Applicants have therefore amended Figs. 4A ad 4B with descriptive labels that are supported in the specification. Withdrawal of the objections are respectfully requested.

On page 3 of the Office Action, the Examiner rejects 1-9 under 35 U.S.C. § 103(a) as being unpatentable over Applicants' admitted prior art (AAPA) in view of Birkett (U.S. Publication 2003/0219067). It is respectfully submitted, however, that the claims are patentable over the art of record for the reasons set forth below.

Birkett teaches up/down conversion circuitry for a radio transceiver. Specifically, the circuitry utilizes a single frequency synthesizer for both the RF and IF stages of the up/down conversion.

Applicants' invention, as recited by claim 1 includes a feature which is neither disclosed nor suggested by the art of record, namely:

> **...wherein the first reference signal is generated independent of the signal output of the frequency multiplier.**

Claim 1 relates to a digital signal receiver which utilizes a reference signal for intermediate frequency conversion, base band conversion and demodulation. The generation of the reference signal is independent of a frequency multiplier used in the receiver. This feature is found in the originally filed application on page 1 and further in Fig. 1. No new matter has been added.

In paragraph 26, Birkett describes a phase lock loop which is shown as loop 100 in Fig. 4. Loop 100 consists of divider 116, multiplier 108, frequency signal 104, low pass filter 112 and Voltage Controlled Oscillator (VCO) 115. This conventional phase lock loop ensures that

the output of the VCO 115 remains constant and does not wander. For example, the output of VCO 115 goes through frequency divider 116 and is then compared to frequency signal 104 via multiplier 108. If a difference between the output of divider 116 and reference signal 104 exists, the output of multiplier 108 will control VCO 115 to adjust its frequency appropriately. This feature is described in Birkett's paragraph 26 ("*the frequency of the output of the voltage controlled oscillator 115 is locked by the loop 100 at a preselected frequency value...based on the value applied to M*"). The reason the output of VCO 115 is divided down by block 116 is because a down conversion is necessary in order to correctly compare the output of VCO 115 with the frequency reference signal 104. Thus, Birkett's output of VCO 115 is generated **dependent** to the output of multiplier 108.

Applicants' claim 1 is different than Birkett, because of the inclusion of the first reference signal being generated **independent** of the output of the frequency multiplier ("*when the first reference signal is generated independent of the signal output of the frequency multiplier*"). Applicants' receiver as shown in Fig. 1 teaches the output of reference signal generator 1 being divided by frequency divider 4. The output of frequency divider 4 is then multiplied by frequency multiplier 5 and then output to OFDM demodulator 6. This structure is different than Birkett because the output of frequency multiplier 5 does not affect reference signal generator 1 (independent). For example, reference signal generator 1 (Birkett's VCO 115) is input to frequency divider 4 (Birkett's frequency divider 116) and then output to frequency multiplier 5 (Birkett's multiplier 108). Applicants frequency multiplier 5, however, is not input to divider 4, and therefore does not affect reference signal generator 1.

On page 4, the Official Action states that it would have be obvious to combine Birkett's loop 100 with AAPA. Applicants respectfully disagree. It would not be obvious to combine the divider 116 and multiplier 108 configuration as taught by Birkett. Birkett teaches a phase lock loop circuit. AAPA does not teach a phase lock loop circuit. Therefore, there would be no motivation to include a divider in AAPA (divider is conventionally not required in circuits such as AAPA). Applicants utilize a divider and multiplier to obtain advantages over conventional circuits. Specifically, Applicants divide and then multiply the reference signal in order to ensure the stability of multiplier 5 and to decrease the power consumption of the receiver. This advantage is described on page 3 lines 22 to page 4 line 3 ("*when the frequency of reference signal from reference signal generator 1 is high, the buffer needs large current to be capable of operating at high frequency...according to the embodiment, the reference signal having the*

divided frequency is input to the frequency multiplier 5...the current of the buffer can be reduced...the frequency multiplier 5 operates stably...consumes a small power").

It is because Applicants include the feature of "*wherein the first reference signal is generated independent of the signal output of the frequency multiplier*", the following advantages are achieved. An advantage is the ability to operate multiplier 5 stably and reduce the amount of power consumed. Accordingly, for the reasons set forth above, claim 1 is patentable over the art of record.

Claims 2-10 include all the features of claim 1 from which they depend. Thus, claims 2-10 are also patentable over the art of record for the reasons set forth above.

New dependent claim 10 has been added to the application. This claim recites the digital signal receiver further comprising a digital demodulator and frequency multiplier. This claim is patentable by virtue of its dependency on allowable claim 7.

...including the digital demodulator and the frequency multiplier.

Support for this claim can be found in the specification as originally filed in Fig. 1. No new matter has been added.

In view of the amendments and arguments set forth above, the above-identified application is in condition for allowance which action is respectfully requested.

Respectfully submitted,

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Attachments: Figures 4A, 4B and 5 (2 sheets)

Dated: January 15, 2008

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